



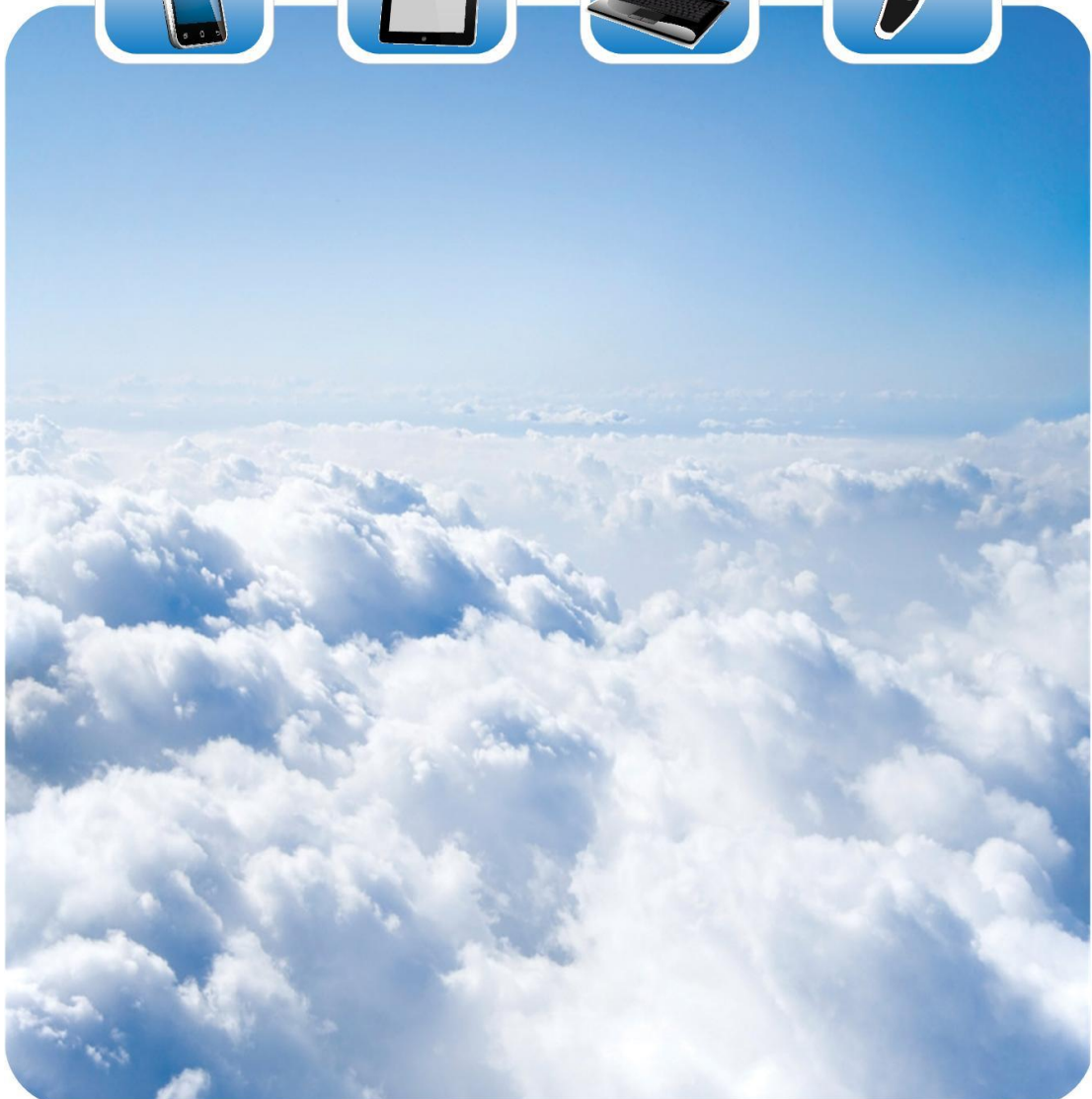
苏州敏芯微电子技术股份有限公司
MEMSensing Microsystems (Suzhou, China) Co., Ltd.

Data Sheet

V 1.0 / Jan. 2016

MSA300

Digital Triaxial Accelerometer



MSA300

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苏州敏芯微电子技术股份有限公司

MEMSensing Microsystems (Suzhou, China) Co., Ltd.



GENERAL DESCRIPTION

MSA300 is a triaxial, low-g accelerometer with I2C/SPI digital output for consumer applications.

It has dynamically user selectable full scales of $\pm 2g/\pm 4g/\pm 8g/\pm 16g$ and allows acceleration measurements with output data rates from 1Hz to 500Hz.

MSA300 is available in an ultra small (2mmx2mm,height 1mm) LGA package and is guaranteed to operate over -40°C to $+85^{\circ}\text{C}$.

FEATURES

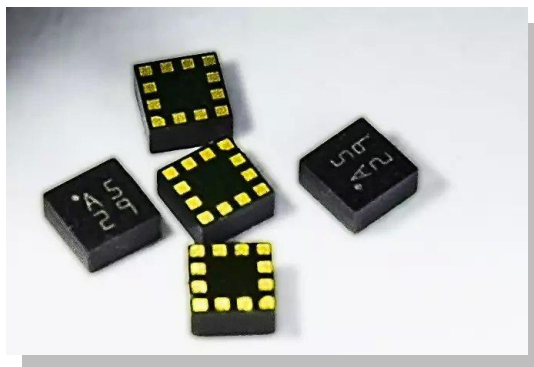
- ✧ Ultra small package 2x2x1 mm LGA-12 pins
- ✧ User selectable range, $\pm 2g$, $\pm 4g$, $\pm 8g$, $\pm 16g$
- ✧ 1.62V to 3.6V supply voltage,
- ✧ 1.2V to 3.6V IO supply voltage
- ✧ User selectable data output rate
- ✧ I2C/SPI(4-wire/3-wire)
- ✧ Two interrupt pins
- ✧ 14 bits resolution
- ✧ Low power consumption

- ✧ Factory programmed offset and sensitivity
- ✧ RoHS compliant

APPLICATIONS

- ✧ User interface for mobile phone and tablet
- ✧ Display orientation
- ✧ Gesture recognition
- ✧ Vibration monitoring
- ✧ Inclination and tilt sensing
- ✧ Pedometer
- ✧ Gaming
- ✧ Free fall detection

PRODUCT VIEW





CONTENTS

| | |
|---|----|
| GENERAL DESCRIPTION..... | 2 |
| FEATURES..... | 2 |
| APPLICATIONS..... | 2 |
| PRODUCT VIEW..... | 2 |
| 1. Pin Description..... | 5 |
| 2. Specification | 6 |
| 2.1 Absolute Maximum Ratings..... | 6 |
| 2.2 Sensor Characteristics..... | 6 |
| 2.3 Electrical Characteristics..... | 7 |
| 3. Function Blocks..... | 8 |
| 4. Functional Description | 9 |
| 4.1 Supply Voltage And Power Management..... | 9 |
| 4.2 Power Modes..... | 9 |
| 4.3 Sensor Data..... | 10 |
| 4.4 Bandwidth..... | 10 |
| 4.5 Interrupt Controller..... | 11 |
| 4.5.1 General fetures..... | 11 |
| 4.5.2 Mapping..... | 12 |
| 4.5.3 Electrical behavior..... | 13 |
| 4.5.4 New data interrupt..... | 13 |
| 4.5.5 Active detection | 13 |
| 4.5.6 Tap detection | 14 |
| 4.5.7 Orientation recognition | 16 |
| 4.5.8 Freefall interrupt..... | 18 |
| 5. Register Map..... | 20 |
| 6. Register Description..... | 21 |
| 7. I2C Interface and Application Collection | 29 |
| 7.1 I2C Interface..... | 29 |
| 7.2 I2C Timing..... | 29 |
| 7.3 I2C Application collection..... | 31 |
| 8. Package Description | 32 |
| 8.1 Outline Dimensions | 32 |

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| | | |
|-----|---------------------------------|----|
| 8.2 | <i>Sensor orientation</i> | 33 |
| 8.3 | <i>Tape and reel</i> | 34 |
| | Revision History | 35 |



1. Pin Description

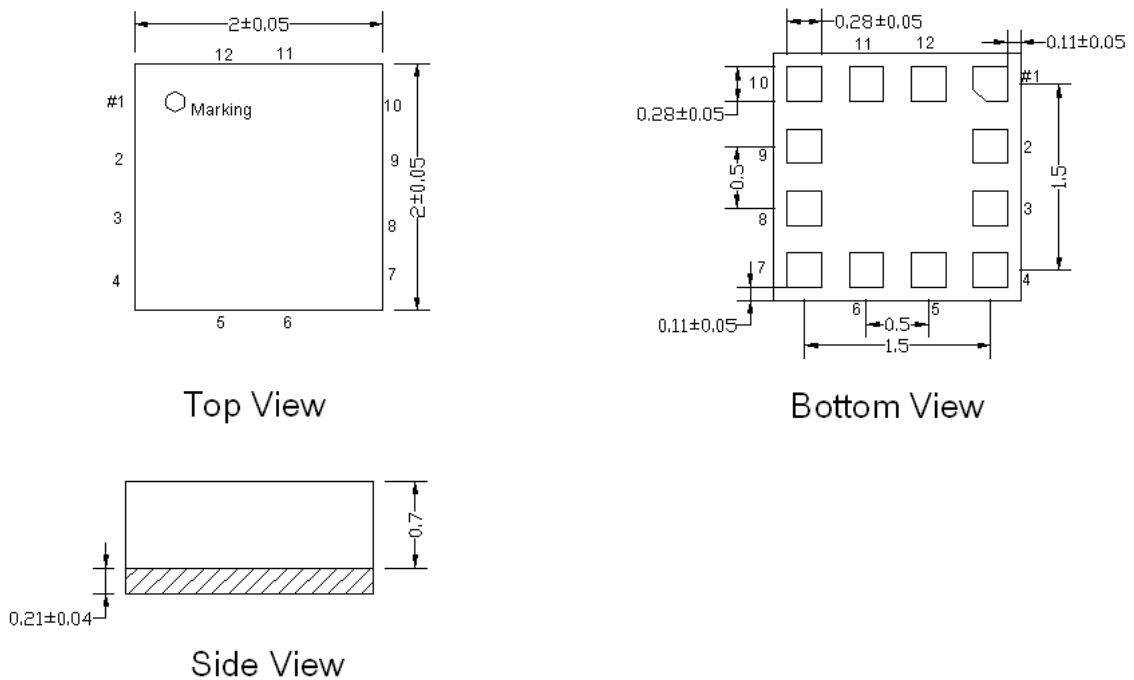


Figure 1: Pin Description

| No. | Name | Function |
|-----|-------|--|
| 1 | SDO | Address for I2C, Data output in SPI(4-wire) mode |
| 2 | SDIO | Data input/output in I2C&SPI(3-wire) mode , Data input in SPI(4-wire) mode |
| 3 | VDDIO | IO Power supply |
| 4 | NC | Connected to GND recommended |
| 5 | INT1 | Interrupt 1 |
| 6 | INT2 | Interrupt 2 |
| 7 | VDD | Power supply |
| 8 | GNDIO | IO ground |
| 9 | GND | Ground |
| 10 | CSB | Chip select in SPI mode |
| 11 | PS | SPI/I2C selection, "1" I2C mode, "0" SPI mode |
| 12 | SCL | Clock for I2C&SPI interface |

Table 1: Absolute Maximum Ratings



2. Specification

2.1 Absolute Maximum Ratings

| Parameter | Maximum value | Unit |
|-----------------------|---------------|------|
| Supply Voltage | -0.3 to 3.6 | V |
| Mechanical Shock | 10,000 | g |
| Operating Temperature | -40 to 85 | °C |
| Storage Temperature | -40 to 125 | °C |

Table 2: Absolute Maximum Ratings

2.2 Sensor Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|---------------------------------------|----------------------------|-----|------|-----|--------|
| FS | Full scale range | | | ±2 | | g |
| | | | | ±4 | | g |
| | | | | ±8 | | g |
| | | | | ±16 | | g |
| S2g | Sensitivity | each axis at 25°C | | 4096 | | LSB/g |
| S4g | | each axis at 25°C | | 2048 | | LSB/g |
| S8g | | each axis at 25°C | | 1024 | | LSB/g |
| S16g | | each axis at 25°C | | 512 | | LSB/g |
| TCS | Sensitivity Temperature Coefficient | FS=±2g | | 0.02 | | %/°C |
| Off | Zero g Offset @ 25 °C, X/Y/Z axis | FS=±2g | | ±80 | | mg |
| TCO | Zero g Offset Temperature Coefficient | FS=±2g, -40 – +85 °C | | ±1 | | mg/°C |
| Nrms | Noise Density | FS=±2g | | 300 | | µg/√Hz |
| NL | Non-Linearity | FS=±2g, best straight line | | 2 | | %FS |
| Cs | Cross Axis Sensitivity | Between any two axes | | 2 | | % |

Table 3: Sensor Characteristics



2.3 Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|---------------------------|----------------------|--------------|-----|--------------|---------------|
| VDD | Supply Voltage | | 1.62 | 1.8 | 3.6 | V |
| VDDIO | IO Supply Voltage | | 1.2 | 1.8 | 3.6 | V |
| IDD | Supply Current | Normal operation | | 180 | | μA |
| IDDpd | | Power down mode | | | 1 | μA |
| IDDlp | | Low Power mode | | | 2 | μA |
| VIL | Voltage input low level | SPI&I2C | | | 0.3VDD IO | V |
| VIH | Voltage input high level | SPI&I2C | 0.7VDD IO | | | V |
| VOL | Voltage output low level | | | | 0.1VDD IO | V |
| VOH | Voltage output high level | | 0.9VDD IO | | | V |
| Twup | Wake up time | From power down mode | | 1 | | ms |
| Tsup | Start up time | From power off | | 3 | | ms |
| BW | Bandwidth | | 1.95 | | 500 | Hz |
| ODR | Output data rate | | 1 | | 1000 | Hz |

Table 4: Sensor Characteristics



3. Function Blocks

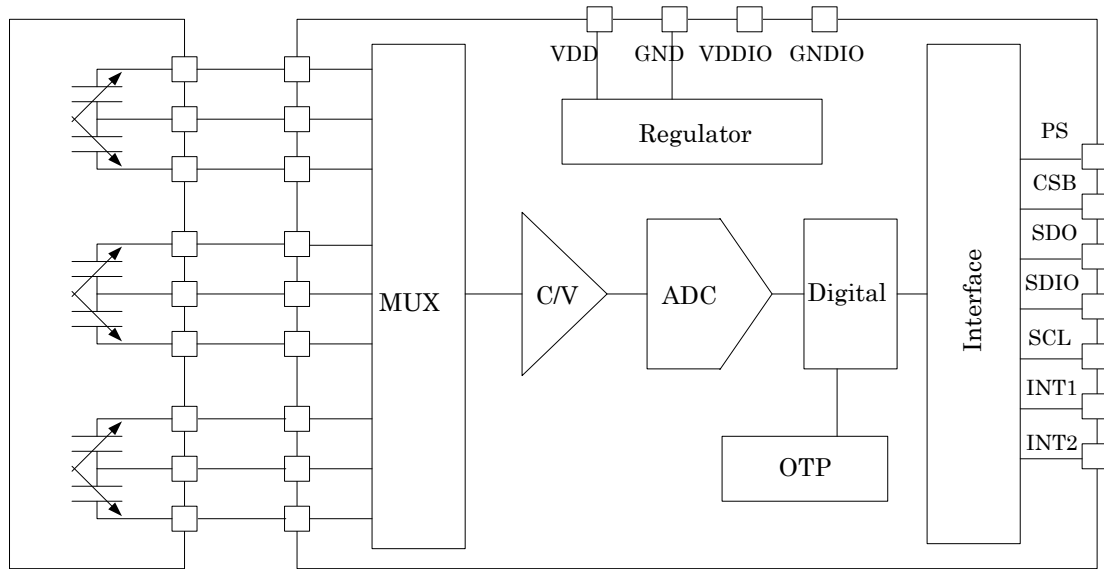


Figure 2: Package Outline Dimensions



4. Functional Description

4.1 Supply Voltage And Power Management

The MSA300 has two distinct power supply pins:

VDD is the main power supply for all internal analog and digital function blocks through several regulators.

VDDIO is a separate power supply pin exclusively used for digital I/O circuits.

There are no limitations on the voltage levels of both pins relative to each other, as long as each of them lies within its operation range. Furthermore the device can be completely switched off (VDD=0V) while keeping the VDDIO supply on (VDDIO>0V).

4.2 Power Modes

The MSA300 has three different power modes. Besides normal mode, which represents the fully operational state of the device, there are two special energy saving modes: low-power mode and suspend mode.

In normal mode:

All parts of the electronic circuit are held powered-up and data acquisition is performed continuously.

In suspend mode:

The whole analog part, oscillators included, is powered down. No data acquisition is performed, the only supported operations are reading registers (latest acceleration data are kept). Suspend mode is entered by writing '11' or '10' to the (0x11) 'POWER_MODE' bits.

In low-power mode:

The device is periodically switching between a sleep phase and a wake-up phase. The wake-up phase essentially corresponds to operation in normal mode with complete power-up of the circuitry. During the sleep phase the analog part ex-



cept the oscillators is powered down. is entered by writing '01' to the 'POWER_MODE' bits.

During the wake-up phase the number of samples required by any enabled interrupt is processed. If an interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary interrupt), or until the interrupt is reset (latched interrupt). If no interrupt is detected, the device enters the sleep phase.

4.3 Sensor Data

The width of acceleration data is 14bits given in two's complement representation. The 14bits for each axis are split into an MSB part (one byte containing bits 13 to 6) and an LSB lower part (one byte containing bits 5 to 0).

The 'NEW_DATA_INT' bit is set when z_axis data is ready. It is reset when register (0x02) or (0x0A) is read. To enable 'NEW_DATA_INT' function, (0x17) 'DATA_INT_EN' should be set.

4.4 Bandwidth

The bandwidth of the acceleration data is always half of the update rate in normal mode and listed in below table.

| ODR | BW |
|--------------------|---------|
| 1000Hz (1010-1111) | 500Hz |
| 500Hz (1001) | 250Hz |
| 250Hz (1000) | 125Hz |
| 125Hz (0111) | 62.5Hz |
| 62.5Hz (0110) | 31.25Hz |
| 31.25Hz (0101) | 15.63Hz |
| 15.63Hz (0100) | 7.81Hz |
| 7.81Hz (0011) | 3.9Hz |
| 3.9Hz (0010) | 1.95Hz |

Table 5: bandwidth under different ODR and BW settings in normal mode

MSA300 supports four different acceleration measurement ranges, it is selected by setting (0x0F) as follows:



| | | | | |
|--------------------|-------|-------|-------|--------|
| Range | 0011 | 0101 | 1000 | 1100 |
| Acceleration range | +/-2g | +/-4g | +/-8g | +/-16g |

Table 6: acceleration measurement range

4.5 Interrupt Controller

Interrupt engines are integrated in the MSA300. Each interrupt can be independently enabled and configured. If the condition of an enabled interrupt is fulfilled, the corresponding status bit is set to 1 and the selected interrupt pin is activated. There are two interrupt pins, INT1 and INT2; interrupts can be freely mapped to any of these two pins. The pin state is a logic 'OR' combination of all mapped interrupts.

4.5.1 General fetures

An interrupt is cleared depending on the selected interrupt mode, which is common to all interrupts. There are three different interrupt modes: non-latched, latched and temporary. The mode is selected by the 'LATCH_INT' bits according to the following table.

| latch_int | Interrupt mode |
|-----------|-------------------------|
| 0000 | non-latched |
| 0001 | temporary latched 250ms |
| 0010 | temporary latched 500ms |
| 0011 | temporary latched 1s |
| 0100 | temporary latched 2s |
| 0101 | temporary latched 4s |
| 0110 | temporary latched 8s |
| 0111 | Latched |
| 1000 | non-latched |
| 1001 | temporary latched 1ms |
| 1010 | temporary latched 1ms |
| 1011 | temporary latched 2ms |



| | |
|------|-------------------------|
| 1100 | temporary latched 25ms |
| 1101 | temporary latched 50ms |
| 1110 | temporary latched 100ms |
| 1111 | Latched |

Table 7: Interrupt mode selection

An interrupt is generated if its activation condition is met. It cannot be cleared as long as the activation condition is fulfilled. In the non-latched mode the interrupt status bit and the selected pin (INT1 or INT2) are cleared as soon as the activation condition is no more valid. Exceptions to this behavior are the new data and orientation, which are automatically reset after a fixed time.

In the latched mode an asserted interrupt status and the selected pin are cleared by writing 1 to bit 'RESET_INT'. If the activation condition still holds when it is cleared, the interrupt status is asserted again with the next change of the acceleration registers.

In the temporary mode an asserted interrupt and selected pin are cleared after a defined period of time. The behavior of the different interrupt modes is shown in the following figure.

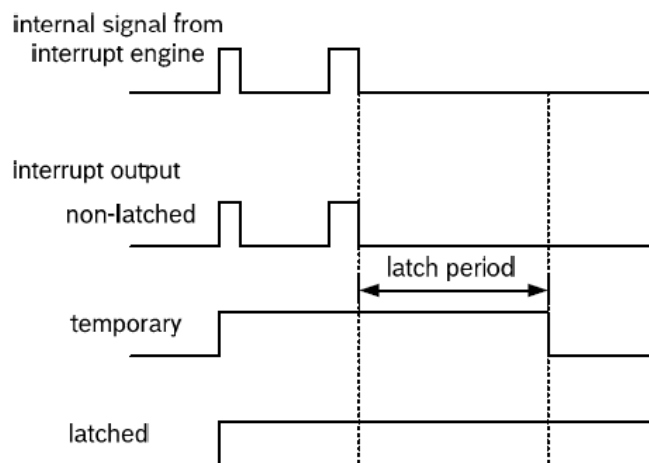


Figure 3: Interrupt mode

4.5.2 Mapping

The mapping of interrupts to the interrupt pins is done by register (0x19, 0x1A,



0x1B), setting `int1_inttype` (`int1_orient/int1_s_tap/int1_freefall`, etc) to 1 can map this type interrupt to INT1 pin and setting `int2_inttype` to 1 can map this type interrupt to INT2 pin.

4.5.3 Electrical behavior

Both interrupt pins can be configured to show desired electrical behavior. The 'active' level of each pin is determined by (0x20) 'INT1_LVL' and (0x20) 'INT2_LVL' bits. If (0x20) 'INT1_LVL' = '1' ('0') / (0x20) 'INT2_LVL' = '1' ('0'), then pin INT1 / pin INT2 is active '1' ('0'). In addition to that, also the electric type of the interrupt pins can be selected. By setting bits (0x20) 'INT1_OD' / (0x20) 'INT2_OD' to '0', the interrupt pin output type gets push-pull, by setting the configuration bits to '1', the output type gets open-drive.

4.5.4 New data interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after an acceleration data was calculated. The interrupt is cleared automatically before the next acceleration data is ready.

4.5.5 Active detection

Active detection uses the slope between successive acceleration signals to detect changes in motion. An interrupt is generated when the slope (absolute value of acceleration difference) exceeds a preset threshold.

The threshold is set with the value of register (0x28) `active_th`, with the LSB corresponding to 16 LSB of acceleration data. That is 3.9mg in 2g-range (7.8mg in 4g-range, 15.6mg in 8g-range and 31.3mg in 16g-range). And the maximum value is 1g in 2g-range, 2g in 4g-range, 4g in 8g-range and 8g in 16g-range.

The time difference between the successive acceleration signals depends is fixed to 1ms.

Active detection can be enabled (disabled) for each axis separately by writing '1' to bits 'ACTIVE_EN_X/Y/Z'. The active interrupt is generated if the slope of any of



the enabled axes exceeds the threshold for $[\text{ACTIVE_DUR}+1]$ consecutive times. As soon as the slopes of all enabled axes fall below this threshold for $[\text{ACTIVE_DUR}+1]$ consecutive times, the interrupt is cleared unless the interrupt signal is latched.

The interrupt status is stored in bit (0x09) 'ACTIVE_INT'. The bit (0x0B) 'ACTIVE_FIRST_X/Y/Z' record which axis triggered the active interrupt first and the sign of this acceleration data that triggered the interrupt is recorded in the bit (0x0B) 'ACTIVE_SIGN'.

4.5.6 Tap detection

Tap detection has a functional similarity with a common laptop touch-pad or clicking keys of a computer mouse. A tap event is detected if a pre-defined pattern of the acceleration slope is fulfilled at least for one axis. Two different tap events are distinguished: A single tap is a single event within a certain time, followed by a certain quiet time. A double tap consists of a first such event followed by a second event within a defined time.

Single tap interrupt is enabled by writing 1 to bit (0x16) 'S_TAP_INT_EN' and double tap interrupt is enabled by writing 1 to bit (0x16) 'D_TAP_INT_EN'. The status of the single tap interrupt is stored in bit (0x09) 'S_TAP_INT' and the status of the double tap interrupt is stored in bit (0x09) 'D_TAP_INT'.

The slope threshold for detecting a tap event is set by bits (0x2B) "TAP_TH" with the LSB corresponding to 256LSB of acceleration data that is 62.5mg in 2g-range, 125mg in 4g-range, 250mg in 8g-range, 500mg in 16g-range. And the maximum value equals to the full scale in each range.

In the following figure the meaning of different timing parameter is visualized.

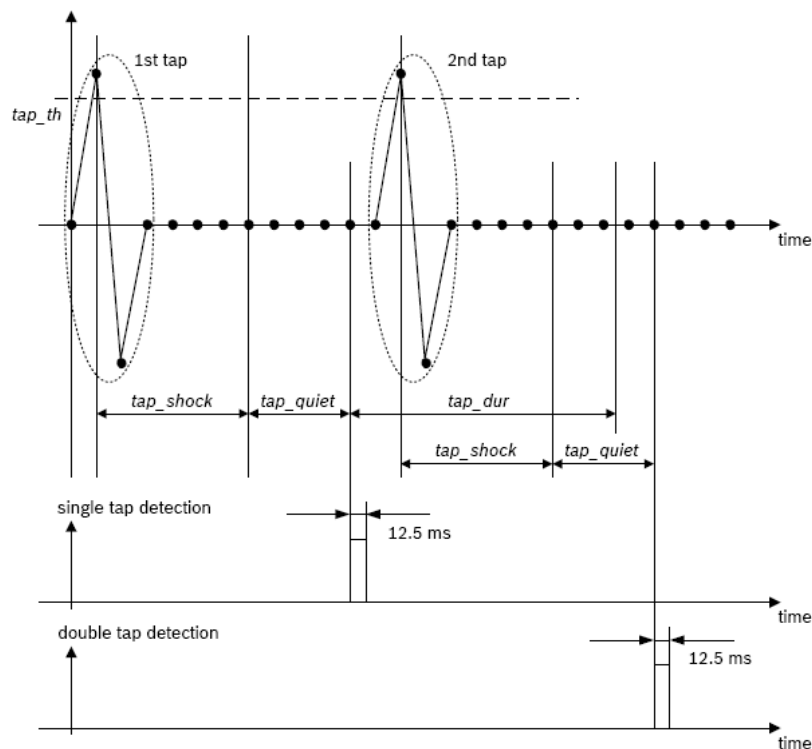


Figure 4: Timing of Tap detection

The parameter (0x2A) 'TAP_SHOCK' and (0x2A) 'TAP_QUIET' apply to both single and double tap detection, while (0x2A) 'TAP_DUR' applies to double detection only. Within the duration of (0x2A) 'TAP_SHOCK' any slope exceeding (0x2B) 'TAP_TH' after the first event is ignored, within the duration of (0x2A) 'TAP_QUIET' there must be no slope exceeding 'TAP_TH', otherwise the first event will be cancelled.

A single tap is detected and the single tap interrupt is generated after the combination durations of (0x2A) 'TAP_SHOCK' and (0x2A) 'TAP_QUIET', if the corresponding slope conditions are fulfilled. The interrupt is cleared after a delay of 12.5ms in non-latched mode.

A double tap is detected and the double tap interrupt is generated if an event fulfilling the conditions for a single tap occurs within the set duration in (0x2A) 'TAP_DUR' after the completion of the first tap event. The interrupt is cleared after a delay of 12.5ms in non-latched mode.

The sign of the slope of the first tap which triggered the interrupt is stored in bit



(0x0B) 'TAP_SIGN' (0 means positive, 1 means negative). The axis which triggered the interrupt is indicated by bits (0x0B) 'TAP_FIRST_X/Y/Z'.

4.5.7 Orientation recognition

The orientation recognition feature informs on an orientation change of sensor with respect to the gravitation field vector 'g'. The measured acceleration vector components with respect to the gravitation field are defined as shown in the following figure.

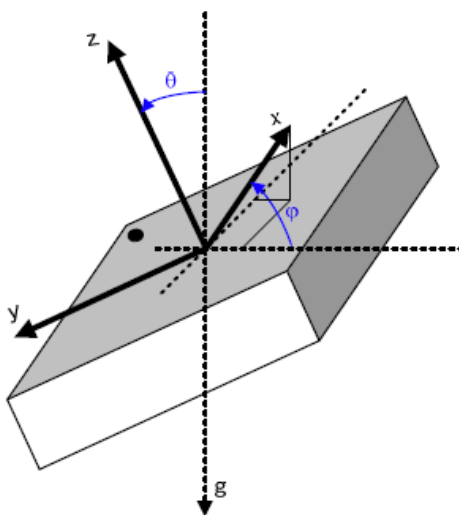


Figure 5: Definition of vector components

Therefore, the magnitudes of the acceleration vectors are calculated as follows:

$$acc_x = 1g \cdot \sin \theta \cdot \cos \varphi$$

$$acc_y = -1g \cdot \sin \theta \cdot \sin \varphi$$

$$acc_z = 1g \cdot \cos \theta$$

Depending on the magnitudes of the acceleration vectors the orientation of the device in the space is determined and stored in the bits (0x0C) 'ORIENT'. There are three orientation calculation modes with different t thresholds for switching between different orientations: symmetrical, high-asymmetrical and low-asymmetrical. The mode is selected by setting the (0x2C) 'ORIENT_MODE' bits. For each orientation mode, the 'ORIENT' bits have a different meaning as show in below table.



| Orient | Name | Angle | Condition |
|--------|----------------------|-----------------------------------|--|
| X00 | Portrait upright | $315^\circ < \varphi < 45^\circ$ | $ \text{acc}_y < \text{acc}_x - \text{'hyst'}$ & $\text{acc}_x \geq 0$ |
| X01 | Portrait upside down | $135^\circ < \varphi < 225^\circ$ | $ \text{acc}_y < \text{acc}_x - \text{'hyst'}$ & $\text{acc}_x < 0$ |
| X10 | Landscape left | $45^\circ < \varphi < 135^\circ$ | $ \text{acc}_y \geq \text{acc}_x + \text{'hyst'}$ & $\text{acc}_y < 0$ |
| X11 | Landscape right | $225^\circ < \varphi < 315^\circ$ | $ \text{acc}_y \geq \text{acc}_x + \text{'hyst'}$ & $\text{acc}_y \geq 0$ |

Table 8: meaning of 'orient' bits in symmetric mode

| Orient | Name | Angle | Condition |
|--------|----------------------|-----------------------------------|--|
| X00 | Portrait upright | $297^\circ < \varphi < 63^\circ$ | $ \text{acc}_y < 2* \text{acc}_x - \text{'hyst'}$ & $\text{acc}_x \geq 0$ |
| X01 | Portrait upside down | $117^\circ < \varphi < 243^\circ$ | $ \text{acc}_y < 2* \text{acc}_x - \text{'hyst'}$ & $\text{acc}_x < 0$ |
| X10 | Landscape left | $63^\circ < \varphi < 117^\circ$ | $ \text{acc}_y \geq 2* \text{acc}_x + \text{'hyst'}$ & $\text{acc}_y < 0$ |
| X11 | Landscape right | $243^\circ < \varphi < 297^\circ$ | $ \text{acc}_y \geq 2* \text{acc}_x + \text{'hyst'}$ & $\text{acc}_y \geq 0$ |

Table 9: meaning of 'orient' bits in high-asymmetric mode

| Orient | Name | Angle | Condition |
|--------|----------------------|-----------------------------------|--|
| X00 | Portrait upright | $333^\circ < \varphi < 27^\circ$ | $ \text{acc}_y < 0.5* \text{acc}_x - \text{'hyst'}$ & $\text{acc}_x \geq 0$ |
| X01 | Portrait upside down | $153^\circ < \varphi < 207^\circ$ | $ \text{acc}_y < 0.5* \text{acc}_x - \text{'hyst'}$ & $\text{acc}_x < 0$ |
| X10 | Landscape left | $27^\circ < \varphi < 153^\circ$ | $ \text{acc}_y \geq 0.5* \text{acc}_x + \text{'hyst'}$ & $\text{acc}_y < 0$ |
| X11 | Landscape right | $207^\circ < \varphi < 333^\circ$ | $ \text{acc}_y \geq 0.5* \text{acc}_x + \text{'hyst'}$ & $\text{acc}_y \geq 0$ |

Table 10: meaning of 'orient' bits in low-asymmetric mode

In the preceding tables, the parameter 'HYST' stands for a hysteresis which can be selected by bits (0x2C) 'ORIENT_HYST'. 1LSB of (0x2C) 'ORIENT_HYST' always corresponds to 62.5mg in any g-range. The MSB of 'orient' bits contains information about the direction of the z-axis. It is set to 0(1) if $\text{acc}_z \geq 0$ ($\text{acc}_z < 0$). The hysteresis for z axis is fixed to 0.2g.

The orient interrupt is enabled by writing (0x16) 'ORIENT_EN' bit. The interrupt is generated if the value of 'orient' has changed. It is automatically cleared after one stable period of the orient value in non-latched mode. In temporary latched or latched mode, the orient value is kept fixed as long as the interrupt



persists. After cleaning the interrupt, the 'ORIENT' will updated with the next following value change.

The change of the 'ORIENT' value and the generation of the interrupt can be blocked according to conditions selected by setting the value of bits (0x2C) 'ORIENT_BLOCKING' as described by below table.

| Orient_blocking | Conditions |
|-----------------|---|
| 00b | No blocking |
| 01b | Z blocking |
| 10b | Z blocking or acceleration slope in any axis > 0.2g |
| 11b | No blocking |

Table 11: blocking conditions for orientation recognition

The Z blocking is defined by the following inequality:

$$|acc_z| > z_blocking$$

The parameter z_blocking of the above given equation stands for the contents of the 'z_blocking' bits. Hereby it is possible to define a blocking value between 0g and 0.9375g with an LSB = 0.0625g.

4.5.8 Freefall interrupt

This interrupt is based on the comparison of acceleration data against a low-g threshold. The interrupt is enabled by writing 1 to the bit (0x17) 'FREEFALL_EN'. There are two modes available: single mode and sum mode. In single mode the acceleration of each axis is compared with the threshold. In sum mode, the sum of absolute values of all accelerations $|acc_x| + |acc_y| + |acc_z|$ is compared with the threshold. The mode is selected by the bit 'FREEFALL_MODE'. The freefall threshold is set through the 'FREEFALL_TH' bits with 1 LSB corresponding to an acceleration of 7.81mg. A hysteresis can be selected by setting the 'FREEFALL_HY' bits with 1 LSB corresponding to 125mg.

The freefall interrupt is generated if the absolute values of the acceleration of all axes or their sum are lower than the threshold for at least the time defined by (0x22) 'FREEFALL_DUR' bits. The interrupt is reset if the absolute value of at

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least one axis or the sum is higher than the threshold plus the hysteresis for at least one data acquisition. The interrupt status is stored in bit (0x09) 'FREEFALL_INT'.



5. Register Map

| Ad- dress | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | De- fault |
|--------------|-------------------|--------------------|------------------|-------------------|----------------------|---------------------|---------------------|---------------------|--------------|
| 0x00 | 4-WIRE | LSB FIRST | SOFT RESET | | | SOFT RESET | LSB FIRST | 4-WIRE | 0x00 |
| 0x01 | PARTID[7:0] | | | | | | | | 0x00 |
| 0x02 | ACC_X[5:0] | | | | | | | | 0x00 |
| 0x03 | ACC_X[13:6] | | | | | | | | 0x00 |
| 0x04 | ACC_Y[5:0] | | | | | | | | 0x00 |
| 0x05 | ACC_Y[13:6] | | | | | | | | 0x00 |
| 0x06 | ACC_Z[5:0] | | | | | | | | 0x00 |
| 0x07 | ACC_Z[13:6] | | | | | | | | 0x00 |
| 0x09 | | ORIENT_INT | S_TAP_INT | D_TAP_IN T | | ACTIVE_INT | | FREEFALL_I NT | 0x00 |
| 0x0A | | | | | | | | NEW_DATA_I NT | 0x00 |
| 0x0B | TAP_SIGN | TAP_FIST_X | TAP_FIRST_ Y | TAP_FIRS T_Z | ACTIVE_SIGN | ACTIVE_FIST _X | ACTIVE_FIST _Y | ACTIVE_FIST _Z | 0x00 |
| 0x0C | ORIENT[2:0] | | | | | | | | 0x00 |
| 0x0D | FIFO_ENTRIES[5:0] | | | | | | | | 0x00 |
| 0x0F | | | | | RESOLUTION[1:0] | | FS[1:0] | | 0x00 |
| 0x10 | X-AXIS_DIS | Y-AXIS_DIS | Z-AXIS_DIS | | ODR[3:0] | | | | 0x0F |
| 0x11 | PWR_MODE | | | LOW_POWER_BW[3:0] | | | | | 0x9E |
| 0x12 | | | | | X_POLARITY | Y_POLARITY | Z_POLARITY | X_Y_SWAP | 0x00 |
| 0x16 | | ORIENT_INT _EN | S_TAP_INT_ EN | D_TAP_IN T_EN | | ACTIVE_INT_ EN_Z | ACTIVE_INT_ EN_Y | ACTIVE_INT_ EN_X | 0x00 |
| 0x17 | | OVERRUN_IN T_EN | | DATA_INT _EN | FREEFALL_IN T_EN | | | | 0x00 |
| 0x19 | | INT1_ORIEN T | INT1_S_TA P | INT1_D_T AP | | INT1_ACTIV E | | INT1_FREEF ALL | 0x00 |
| 0x1A | INT2_NEW_ DATA | | INT2_OVER RUN | | | INT1_OVERR UN | | INT1_NEW_ DATA | 0x00 |
| 0x1B | | INT2_ORIEN T | INT2_S_TA P | INT2_D_T AP | | INT2_ACTIV E | | INT2_FREEF ALL | 0x00 |
| 0x20 | | | | | INT2_OD | INT2_LVL | INT1_OD | INT1_LVL | 0x00 |
| 0x21 | RESET_INT | | | | LATCH_INT[3:0] | | | | 0x00 |
| 0x22 | FREEFALL_DUR[7:0] | | | | | | | | 0x09 |
| 0x23 | FREEFALL_TH[7:0] | | | | | | | | 0x30 |
| 0x24 | | | | | | FREEFALL_ MODE | FREEFALL_HY[1:0] | | 0x01 |
| 0x27 | | | | | | | ACTIVE_DUR[1:0] | | 0x00 |
| 0x28 | ACTIVE_TH | | | | | | | | 0x14 |
| 0x2A | TAP_QUIET | TAP_SHOCK | | | | TAP_DUR[2:0] | | | 0x04 |
| 0x2B | | | | | TAP_TH[4:0] | | | | 0x0A |
| 0x2C | ORIENT_HYST[2:0] | | | | ORIENT_BLOCKING[1:0] | | ORIENT_MODE[1:0] | | 0x18 |
| 0x2D | Z_BLOCKING[3:0] | | | | | | | | 0x08 |
| 0x38 | OFFSET_X[7:0] | | | | | | | | 0x00 |
| 0x39 | OFFSET_Y[7:0] | | | | | | | | 0x00 |
| 0x3A | OFFSET_Z[7:0] | | | | | | | | 0x00 |



6. Register Description

Register 0x00(Soft Reset) :Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|--------|--------------|---------------|------|------|------------|--------------|--------|---------|
| 4-wire | LSB First | Soft Reset | | | Soft Reset | LSB First | 4-wire | 0X00 |

Soft Reset: 0:soft reset disable, 1:soft reset enable

Reg 0x01(PartID):Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|-------------|------|------|------|------|------|------|------|---------|
| PARTID[7:0] | | | | | | | | 0X00 |

Reg 0x02/0x03(X_axis Data LSB/MSB) :Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|-------------|------|------|------|------|------|------|------|---------|
| ACC_X[5:0] | | | | | | | | 0X00 |
| Acc_x[13:6] | | | | | | | | 0X00 |

Reg 0x04/0x05(Y_axis Data LSB/MSB) :Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|-------------|------|------|------|------|------|------|------|---------|
| ACC_Y[5:0] | | | | | | | | 0X00 |
| ACC_Y[13:6] | | | | | | | | 0X00 |

Reg 0x06/0x07(Z_axis Data LSB/MSB) :Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|-------------|------|------|------|------|------|------|------|---------|
| ACC_Z[5:0] | | | | | | | | 0X00 |
| ACC_Z[13:6] | | | | | | | | 0X00 |

Reg 0x09(Motion_Interrupt) :Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------------|-----------|-----------|------|------------|------|--------------|---------|
| | ORIENT_INT | S_TAP_INT | D_TAP_INT | | ACTIVE_INT | | FREEFALL_INT | 0X00 |

ORIENT_INT: orientation interrupt status,0:inactive,1:active

S_TAP_INT: single tap interrupt status,0:inactive,1:active

D_TAP_INT: double tap interrupt status,0:inactive,1:active



ACTIVE_INT: active interrupt status,0:inactive,1:active

FREEFALL_INT: freefall interrupt status,0:inactive,1:active

Reg 0x0A(Data_Interrupt) :Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|------|------|------|------|--------------|---------|
| | | | | | | | NEW_DATA_INT | 0X00 |

NEW_DATA_INT: new data interrupt status,0:inactive,1:active

Reg 0x0B(Tape_Active_Status) :Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|--------------|-----------------|-----------------|-----------------|-----------------|--------------------|--------------------|--------------------|---------|
| TAP_SI GN | TAP_FIR ST_X | TAP_FIR ST_Y | TAP_FIR ST_Z | ACTIVE_ SIGN | ACTIVE_FI RST_X | ACTIVE_FI RST_Y | ACTIVE_F IRST_Z | 0X00 |

TAP_SIGN: sign of tap triggering signal, 0:positive,1:negative

TAP_FIRST_X: tap interrupt triggered by x axis, 1:positive,0:negative

TAP_FIRST_Y: tap interrupt triggered by y axis, 1:positive,0:negative

TAP_FIRST_Z: tap interrupt triggered by z axis, 1:positive,0:negative

ACTIVE_SIGN: sign of active interrupt, 0:positive,1:negative

ACTIVE_FIRST_X: active interrupt triggered by x axis, 1:positive,0:negative

ACTIVE_FIRST_Y: active interrupt triggered by y axis, 1:positive,0:negative

ACTIVE_FIRST_Z: active interrupt triggered by z axis, 1:positive,0:negative

Reg 0x0C(Orientation_Status) :Read only

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|-------------|------|------|------|------|------|------|---------|
| | ORIENT[2:0] | | | | | | | 0X00 |

ORIENT[2]: orientation value of z axis, 0:upward looking, 1:downward looking

ORIENT[1:0]: orientation value of x/y axes

00:portrait upright, 01:portrait upsidedown

10:landscape left, 11:landscape right

Reg 0x0F(Resolution/Range): Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|------|-----------------|------|---------|------|---------|
| | | | | RESOLUTION[1:0] | | FS[1:0] | | 0X00 |

RESOLUTION[1:0]: resolution of x/y/z axes, 00:14bit, 01:12bit, 10:10bit, 11:8bit

RANGE[1:0]: acceleration range of x/y/z axes, 00:+/-2g, 01:+/-4g, 10:+/-8g, 11:+/-16g

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Reg0x10(ODR) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------------|------------|------------|------|----------|------|------|------|---------|
| X_AXIS_DIS | Y_AXIS_DIS | Z_AXIS_DIS | | ODR[3:0] | | | | 0X0F |

X_AXIS_DIS: 0:enable, 1:disable

Y_AXIS_DIS: 0:enable, 1:disable

Z_AXIS_DIS: 0:enable, 1:disable

ODR[3:0]: 0000:1Hz (not available in normal mode)

0001:1.95Hz (not available in normal mode)

0010:3.9Hz

0011:7.81Hz

0100:15.63Hz

0101: 31.25Hz

0110: 62.5Hz

0111: 125Hz

1000: 250Hz

1001: 500Hz (not available in low power mode)

1010-1111:1000Hz (not available in low power mode)

Reg0x11(Power Mode/Bandwidth) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|----------|------|------|-------------------|------|------|------|------|---------|
| PWR_MODE | | | LOW_POWER_BW[3:0] | | | | | 0X9E |

PWR_MODE: 00:normal mode, 01:low power mode, 10/11 suspend mode

LOW_POWER_BW[3:0]: 0000-0010:1.95Hz 0011:3.9Hz, 0100:7.81Hz

0101:15.63Hz, 0110: 31.25Hz, 0111: 62.5Hz,

1000: 125Hz, 1001: 250Hz, 1010-1111:500Hz

Reg 0x12(Swap_Polarity) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|------|------------|------------|------------|----------|---------|
| | | | | X_POLARITY | Y_POLARITY | Z_POLARITY | X_Y_SWAP | 0X00 |

X_POLARITY: the polarity of X axis, 0:not reverse, 1:reverse

Y_POLARITY: the polarity of Y axis, 0:not reverse, 1:reverse

Z_POLARITY: the polarity of Z axis, 0:not reverse, 1:reverse

X_Y_SWAP: output of X/Y axis, 0:not swap, 1:swap

**Reg 0x16(Int_Set_0) : Read/Write**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|---------------|--------------|--------------|------|-----------------|-----------------|-----------------|---------|
| | ORIENT_INT_EN | S_TAP_INT_EN | D_TAP_INT_EN | | ACTIVE_INT_EN_Z | ACTIVE_INT_EN_Y | ACTIVE_INT_EN_X | 0X00 |

ORIENT_INT_EN: orient interrupt, 0:disable, 1:enable

S_TAP_INT_EN: single tap interrupt, 0:disable, 1:enable

D_TAP_INT_EN: double tap interrupt, 0:disable, 1:enable

ACTIVE_INT_EN_Z: active interrupt for the z axis, 0:disable, 1:enable

ACTIVE_INT_EN_Y: active interrupt for the y axis, 0:disable, 1:enable

ACTIVE_INT_EN_X: active interrupt for the x axis, 0:disable, 1:enable

Reg 0x17(Int_Set_1) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|-------------|-----------------|------|------|------|---------|
| | | | DATA_INT_EN | FREEFALL_INT_EN | | | | 0X00 |

NEW_DATA_INT_EN: new data interrupt, 0:disable, 1:enable

FREEFALL_INT_EN: freefall interrupt, 0:disable, 1:enable

Reg 0x19(Int_Map_0) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|-------------|------------|------------|------|-------------|------|---------------|---------|
| | INT1_ORIENT | INT1_S_TAP | INT1_D_TAP | | INT1_ACTIVE | | INT1_FREEFALL | 0X00 |

INT1_ORIENT: map orientation interrupt to INT1, 0:disable, 1:enable

INT1_S_TAP: map single tap interrupt to INT1, 0:disable, 1:enable

INT1_D_TAP: map double tap interrupt to INT1, 0:disable, 1:enable

INT1_ACTIVE: map active interrupt to INT1, 0:disable, 1:enable

INT1_FREEFALL: map freefall interrupt to INT1, 0:disable, 1:enable

Reg 0x1A(Int_Map_1) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|---------------|------|------|------|------|------|------|---------------|---------|
| INT2_NEW_DATA | | | | | | | INT1_NEW_DATA | 0X00 |

INT2_NEW_DATA: map new data interrupt to INT2, 0:disable, 1:enable

INT1_NEW_DATA: map new data interrupt to INT1, 0:disable, 1:enable

Reg 0x1B(Int_Map_2) : Read/Write



| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|-----------------|----------------|----------------|------|-----------------|--------------|-------------------|---------|
| | INT2_ORI ENT | INT2_S_T AP | INT2_D_ TAP | | INT2_ACTI VE | RESERVE D | INT2_FR EEFALL | 0X00 |

INT2_ORIENT: map orientation interrupt to INT2, 0:disable, 1:enable

INT2_S_TAP: map single tap interrupt to INT2, 0:disable, 1:enable

INT2_D_TAP: map double tap interrupt to INT2, 0:disable, 1:enable

INT2_ACTIVE: map active interrupt to INT2, 0:disable, 1:enable

INT2_FREEFALL: map freefall interrupt to INT2, 0:disable, 1:enable

Reg 0x20 (Int_Map_2) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|------|---------|----------|---------|----------|---------|
| | | | | INT2_OD | INT2_LVL | INT1_OD | INT1_LVL | 0X00 |

INT2_OD: select output for INT2, 0: push-pull, 1:OD

INT2_LVL: select active level for INT2, 0: low, 1:high

INT1_OD: select output for INT1, 0: push-pull, 1:OD

INT1_LVL: select active level for INT1, 0: low, 1:high

Reg 0x21 (Int_Latch) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|-----------|------|------|------|----------------|------|------|------|---------|
| RESET_INT | | | | LATCH_INT[3:0] | | | | 0X00 |

RESET_INT: reset or not, 1: reset all latched int, 0:not reset all latched int

LATCH_INT[3:0]: 0000: non-latched

0001: tempoary latched 250ms

0010: tempoary latched 500ms

0011: tempoary latched 1s

0100: tempoary latched 2s

0101: tempoary latched 4s

0110: tempoary latched 8s

0111: latched

1000: non-latched

1001: tempoary latched 1ms

1010: tempoary latched 1ms

1011: tempoary latched 2ms

1100: tempoary latched 25ms

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1101: temporary latched 50ms

1110: temporary latched 100ms

1111: latched

Reg 0x22 (Freefall_Dur) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|-------------------|------|------|------|------|------|------|------|---------|
| FREEFALL_DUR[7:0] | | | | | | | | 0X09 |

FREEFALL_DUR[7:0]: delay_time is (FREEFALL_DUR[7:0] +1) ×2ms, range from 2ms to 512ms, the default delay time is 20ms

Reg 0x23 (Freefall_Th) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------------------|------|------|------|------|------|------|------|---------|
| FREEFALL_TH[7:0] | | | | | | | | 0X30 |

FREEFALL_TH[7:0]: threshold value is freefall_th[7:0] ×7.81mg, default value is 375mg

Reg 0x24 (Freefall_Hy) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|------|------|---------------|------------------|------|---------|
| | | | | | FREEFALL_MODE | FREEFALL_HY[1:0] | | 0X01 |

FREEFALL_MODE: 0. single mode. 1,sum_mode..

FREEFALL_HY[1:0]: freefall hysteresis time is FREEFALL_HY[1:0] ×125mg

Reg 0x27 (Active_Dur) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|------|------|------|-----------------|------|---------|
| | | | | | | ACTIVE_DUR[1:0] | | 0X00 |

ACTIVE_DUR[1:0]: active duration time is (ACTIVE_DUR[1:0]+1)ms

Reg 0x28(Active_Th) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|----------------|------|------|------|------|------|------|------|---------|
| ACTIVE_TH[7:0] | | | | | | | | 0X14 |

ACTIVE_TH[7:0]: threshold of active interrupt

3.91mg/LSB(2g range)

7.81mg/LSB(4g range)

15.625mg/LSB(8g range)

31.25mg/LSB(16g range)



Reg 0x2A(Tap_Dur) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|-----------|-----------|------|------|------|--------------|------|------|---------|
| TAP_QUIET | TAP_SHOCK | | | | TAP_DUR[2:0] | | | 0X04 |

TAP_QUIET: 0: tap quiet duration 30ms, 1: tap quiet duration 20ms

TAP_SHOCK: 0: tap shock duration 50ms, 1: tap shock duration 70ms

TAP_DUR[2:0]: selects the length of the time window for the second shock

000: 50ms. 001: 100ms

010: 150ms. 011: 200ms

100: 250ms, 101: 375ms

110: 500ms, 111: 700ms

Reg 0x2B(Tap_Th) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|-------------|------|------|------|------|---------|
| | | | TAP_TH[4:0] | | | | | 0X0a |

TAP_TH[4:0]: threshold of tap interrupt.

62.5mg/LSB(2g range)

125mg/LSB(4g range)

250mg/LSB(8g range)

500mg/LSB(16g range)

Reg 0x2C(Orient_Hy) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------------------|------|------|----------------------|------|------------------|------|---------|
| | ORIENT_HYST[2:0] | | | ORIENT_BLOCKING[2:0] | | ORIENT_MODE[2:0] | | 0X18 |

ORIENT_HYST[2:0]: set the hysteresis of the orientation interrupt, 1LSB is 62.5mg.

ORIENT_BLOCK[1:0]: select the block mode

00: no blocking

01: z_axis blocking

10: z_axis blocking or slope in any axis > 0.2g

11: no blocking

ORIENT_MODE[1:0]: set the thresholds

00: symmetrical

01: high-asymmetrical

10: low-asymmetrical

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11:symmetrical

Reg 0x2D(Z_Block) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|------|------|------|------|------|-----------------|------|------|---------|
| | | | | | Z_BLOCKING[3:0] | | | 0X08 |

Z_BLOCK[3:0]: defines the block acc_z between 0g to 1g

Reg 0x38/0x39/0x40 (Offset_compensation) : Read/Write

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Default |
|---------------|------|------|------|------|------|------|------|---------|
| OFFSET_X[7:0] | | | | | | | | 0X00 |
| OFFSET_Y[7:0] | | | | | | | | 0X00 |
| OFFSET_Z[7:0] | | | | | | | | 0X00 |

OFFSET_X[7:0]: the offset compensation value for X axis, 1LSB is 3.9mg

OFFSET_Y[7:0]: the offset compensation value for Y axis, 1LSB is 3.9mg

OFFSET_Z[7:0]: the offset compensation value for Z axis, 1LSB is 3.9mg



7. I2C Interface and Application Collection

7.1 I2C Interface

I2C bus uses SCL and SDIO as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free.

The I2C device address of MSA300 is shown as following table. The LSB bit of the 7bits device address is configured via SDO pin.

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | W/R |
|------|------|------|------|------|------|------|-----|
| 0 | 1 | 0 | 0 | 1 | 1 | SDO | 0/1 |

Table 12: I2C Address.

| | | |
|---------------|----------|----------------------------|
| I2C Address : | 01001100 | SDO pulled to GND, Write |
| | 01001101 | SDO pulled to GND, Read |
| | 01001110 | SDO pulled to VDDIO, Write |
| | 01001111 | SDO pulled to VDDIO, Read |

7.2 I2C Timing

| Symbol | Parameter | Condition | Min | Max | Unit |
|------------------|---|-----------|-----|-----|------|
| f_{scl} | Clock frequency | | | 400 | kHz |
| t_{scl_l} | SCL low pulse | | 1.3 | | us |
| t_{scl_h} | SCL high pulse | | 0.6 | | us |
| T_{sda_setup} | SDA setup time | | 0.1 | | us |
| T_{sda_hold} | SDA hold time | | 0.0 | | us |
| t_{susta} | Setup Time for a repeated start condition | | 0.6 | | us |
| t_{hdsta} | Hold time for a start condi- | | 0.6 | | us |



| | tion | | | |
|--------------------|--|--|-----|----|
| t_{susto} | Setup Time for a stop condition | | 0.6 | us |
| t_{buf} | Time before a new transmission can start | | 1.3 | us |

Table 13: Electrical specification of the I2C interface pins

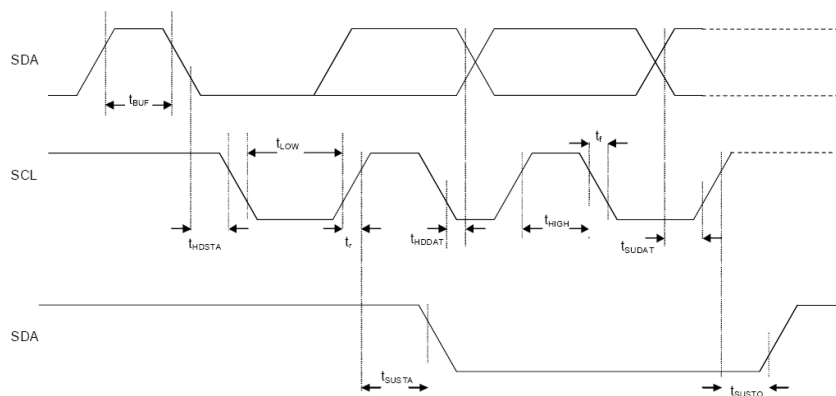


Figure 6: I2C Timing Diagram

The I2C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

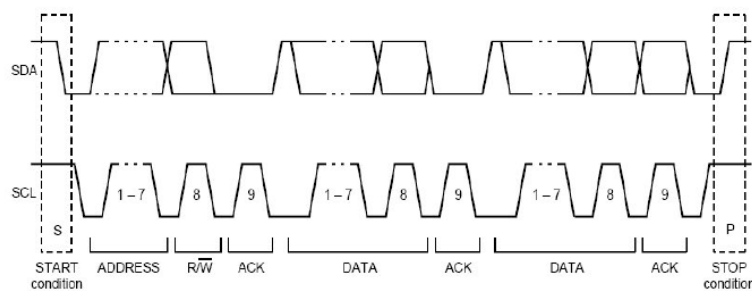


Figure 7: I2C Protocol



7.3 I2C Application collection

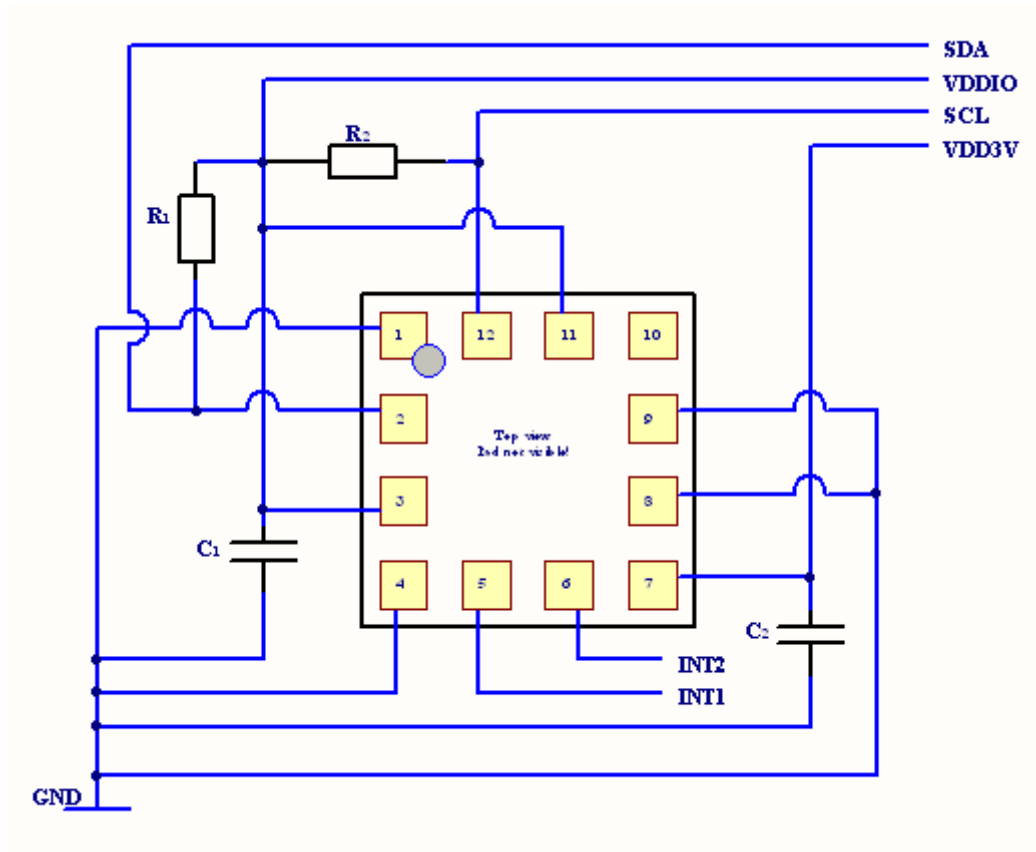


Figure 8: I2C application electrical collection

Note:

The recommended value for C1, C2 is 100nF.

The typical value for R1,R2 is 4.7k Ω pull up resistors.



8. Package Description

8.1 Outline Dimensions

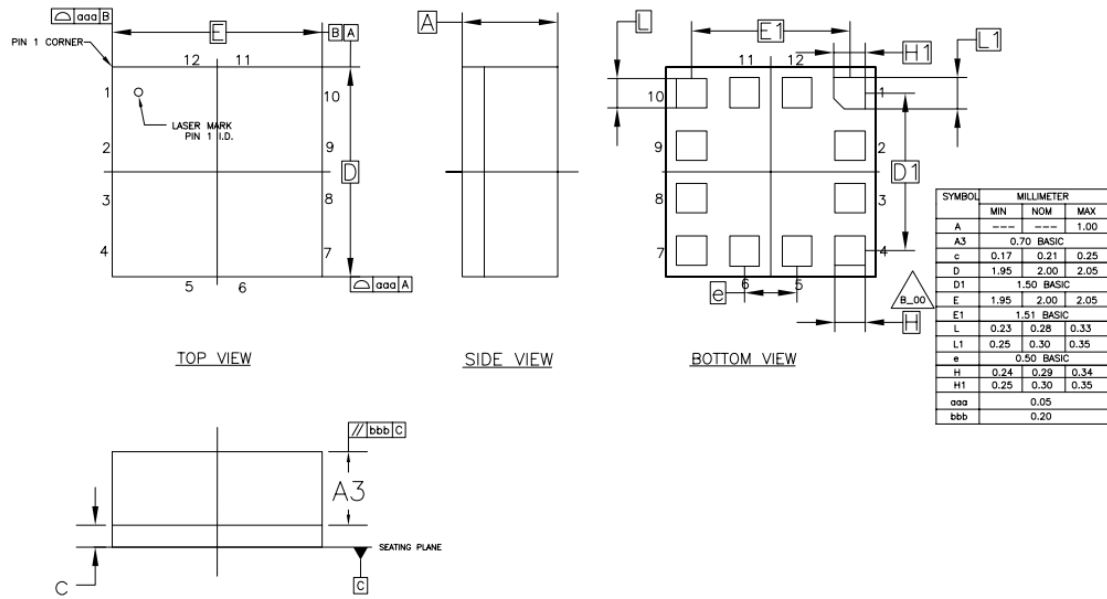


Figure 9: Package Pin Dimensions



8.2 Sensor orientation

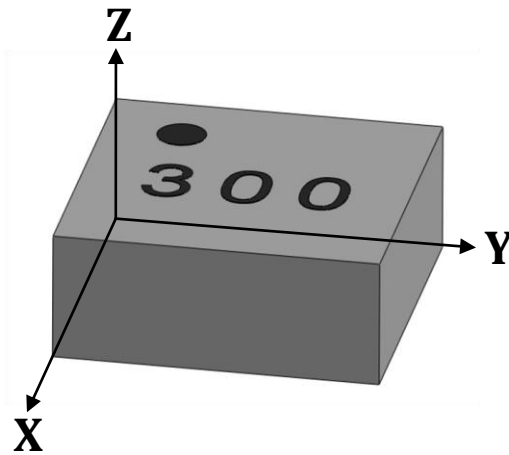
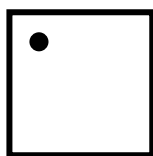
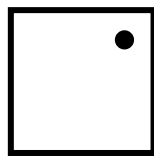


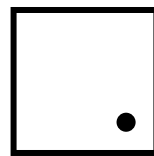
Figure 10: Orientation of sensing axis



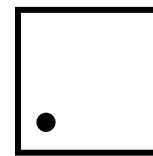
X axis:1g
Y axis:0g
Z axis:0g



X axis:0g
Y axis:1g
Z axis:0g



X axis:-1g
Y axis:0g
Z axis:0g



X axis:0g
Y axis:-1g
Z axis:0g



X axis:0g
Y axis:0g
Z axis:1g

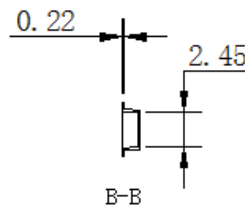
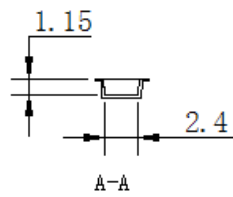
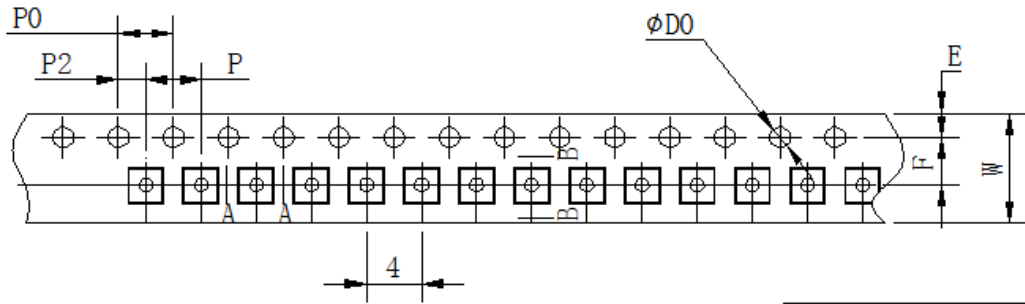


X axis:0g
Y axis:0g
Z axis:-1g

Figure 11: Output signal of sensing axis orientation



8.3 Tape and reel



| Size | |
|------------|--|
| E | 1.75 ± 0.10 |
| F | 5.50 ± 0.10 |
| P2 | 2.00 ± 0.10 |
| ϕD_0 | 1.50 ^{+0.10} _{-0.00} |
| $\phi D1$ | 1.20 ± 0.10 |
| P_0 | 4.00 ± 0.10 |
| 10 P_0 | 40.00 ± 0.20 |
| W | 8.00 ± 0.30 |
| P | 4.00 ± 0.10 |
| A_0 | 2.40 ± 0.10 |
| B0 | 2.45 ± 0.10 |
| K0 | 1.15 ± 0.10 |
| t | 0.22 ± 0.05 |

Figure 12: Tape and reel dimension in mm

MSA300

Digital Triaxial Accelerometer



苏州敏芯微电子技术股份有限公司

MEMSensing Microsystems (Suzhou, China) Co., Ltd.



Revision History

| Revision | Subjects (major changes since last revision) | Date |
|----------|--|-----------|
| 1.0 | Initial Release | 2016-1-13 |
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